

Figure 1

34 Mux Control Registers

17

Bit #	D3	D2	D1	D0
Bit Name (Read)	m_reset_n	Grant	peer_req	req
Bit Name (Write)	m_reset_n	N/A	mux_x_ovrd	req

27

Bit #	D3	D2	D1	D0
Bit Name (Read)	m_reset_n	Grant	peer_req	req
Bit Name (Write)	m_reset_n	N/A	mux_x_ovrd	req

Figure 2

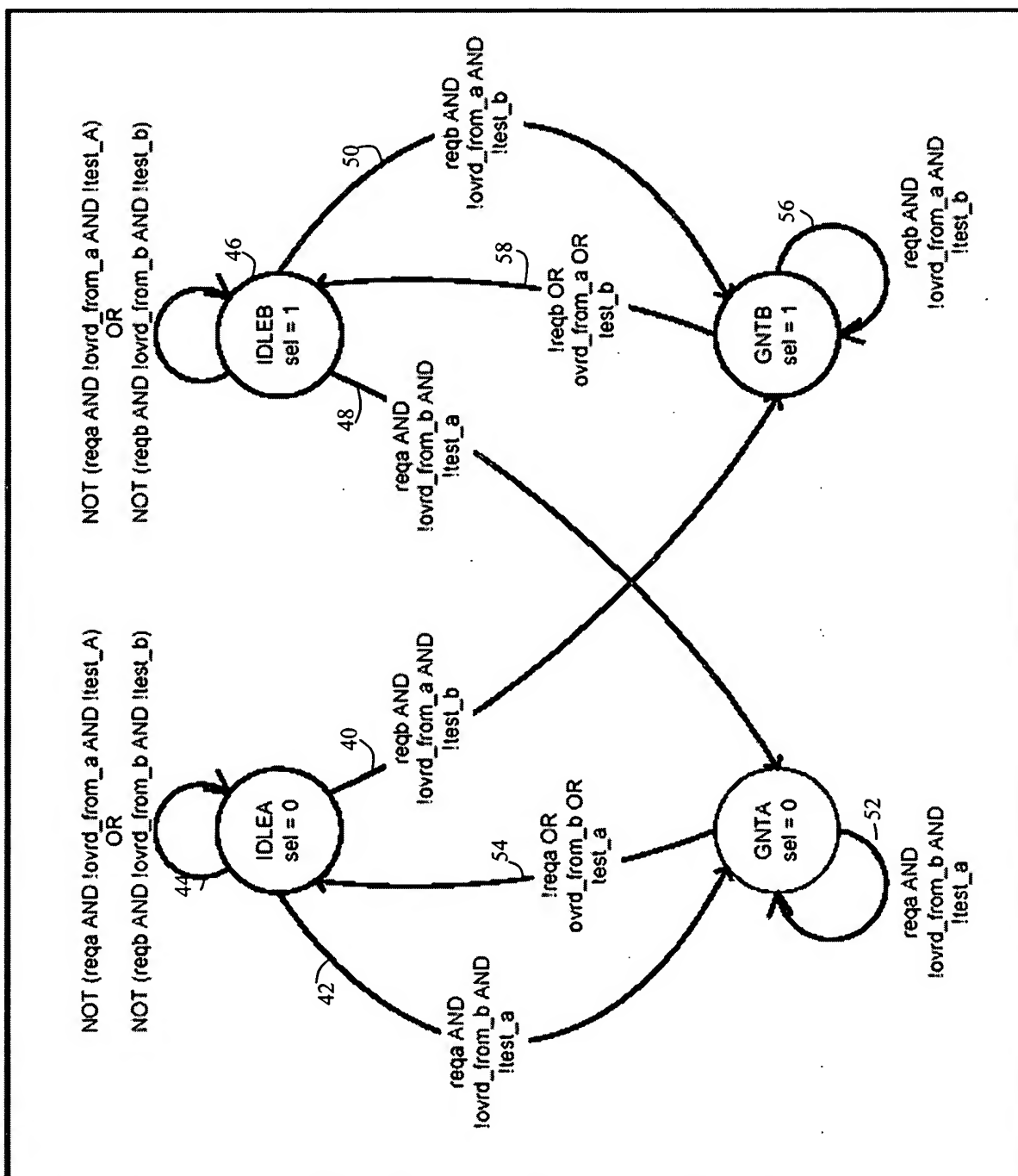


Figure 3